Memory Mapper

Original article (reviewed CPU-MSX no 34 and 35)
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PART 1 - THE OPERATION OF MAPPER

A lot of times the user buys games or programs, but after several attempts of trying them, end up thinking that his/her personal computer is defective.

However, after other tests, they verify that his/her equipment is working perfectly. He/she appears the indignation and revolt then, because when returning to the softwarehouse to complain, it receives an irritating response: His/her personal computer doesn't have a Memory Mapper and without that expansion the programs will never turn. With that the user is questioned if it is worthwhile to buy more expansion of memory, very similar to MegaRAM, the users' of MSX old acquaintance. The truth, however, it is that that “new” expansion is the true expansion of memory for MSX. To proceed we will enumerate some advantages of possessing a Memory Mapper internally:
Memory Mapper follows the standard precisely of MSX, being recognised by the system as real expansion of memory, what doesn't happen with MegaRAM.
It doesn't occupy the external slots, already so scarce our personal computers.
It is used by 95% of the European programs, that you/they are countless and not just a half dozen, as it is the case of MegaRAM. Among them we can highlight the following ones:
Dynamic Publisher
Ease
Final Graphics
Video Graphic Philips
The Animator
All of the games of MegaROM are already adapted for Mapper. Good part of these games, besides programs, we have and utilities already are available in Brazil.
Many games of MegaROM (from where arose MegaRAM) they use sound interfaces different from PSG (internal sound chip of MSX) as it is the case of Konami, that uses SCC, and of other manufacturers that use FM. But with MegaRAM it is impossible to use such interfaces since the two external slots of the personal computer are busy (one with MegaRAM and other with the drive interface). Already with Mapper internally such an inconvenient one doesn't happen, therefore there is a free slot in which we can connect a cartridge of SCC or of FM, allowing to hear the original soundtrack. Mapper can be manipulated in Basic, thing that no and possible with MegaRAM. - Its access is fast, easy and efficient as it was already described in previous remarks. Since Memory Mapper described in this article is installed internally, a good part of the necessary circuit to the assembly of Mapper is already contained in the own personal computer. With this, the number of components is reduced drastically and consequently, cost.

1.1) DESCRIPTION OF THE PROJECT

Our project is a Memory Mapper of 256 Kbyte, installed internally, for personal computers MSX2 and MSX2+, that it will occupy the slot of the bank of RAM of 64 Kbyte, substituting it for another of 256 Kbyte. Can the user be wondering why just in MSX2 and MSX2+? The response is simple: the BIOS (ROM) of these personal computers boots Memory Mapper's records, without which a beautiful crash would happen in the system with certainty. The BIOS of MSX 2+ still goes further, showing us with initialisation the size of Mapper with the message “Main RAM: size.” In our case: “Main RAM: 256Kbytes.”
Memory Mapper divides the bank of 256 Kbyte in 16 blocks of 16 Kbyte each and to manage these blocks, it has 4 records (R0 R3), of 8 bits each. For 256Kb, these records can contain a number from 0 to 15, that corresponds to the number of blocks of the bank of RAM, what means that only 4 bits will be used. CPU accesses the records through ports in which we can read or write:

Record	**Ports of access**	**Page**
R0	FCH	P. 1
R1	FDH	P. 2
R2	FEH	P. 3
R3	FFH	P. 4

Each one of the four records is responsible for the management of a page of memory.
So that a certain record of Mapper appears for a certain block of the bank of 256 Kb is enough to write in the port of access of the respective record the number of the block to be “mapped.”
For instance, we will suppose that the user wants the page 01 of memory to be the block number 08 of the bank of 256 Kb. The responsible for the “mapping” of the page 01 it is the record R1 of Mapper and its access port is FDH. Therefore it is enough the user to write in this port the number of the block:

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OUT &HFD, 08H
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In an MSX without Mapper internally the address lines A15 and A14 do the selection of the pages of memory:

A15	**A14**	**Page**
0	0	P. 0
0	1	P. 1
0	0	P. 2
1	1	P. 3

With Mapper internally installed, the lines A15 and A14 start to select the records of Mapper (R0 R3) that select the blocks of the bank of 256 Kb for its time.

A15	A14	**Record**
0	0	R0
0	1	R1
0	0	R2
1	1	R3

1.2) THE PROJECT HOW IT WORKS

In the Illustration 1 we have the diagram in blocks of Memory Mapper interns of 256 Kbyte. In this illustration we can notice that the basic circuit of Mapper possesses:
a decoder of I/O (Dec)
four registers (Regs)
a multiplexador (MPX)
an auxiliary circuit of Refresh (AuxRfsh)

COMPONENTS:

IC's

IC l	74LS30
IC 2	74LS138
IC 3 AND IC4	74LS670
IC5	74LS153
IC6	74LS74

RAM

Eight dynamic memory chips of 256Kb x 1 bit that can be: KM41256, GMC71256, ICM41256, TM50256 or TSM4256.

Other

Connector "new [Latch]" as of 50 roads.
Flat Cable as of 50 roads (10 the one 14[cm])
Thread "ware up" about to connect among the ICs.
Bread / Strip board

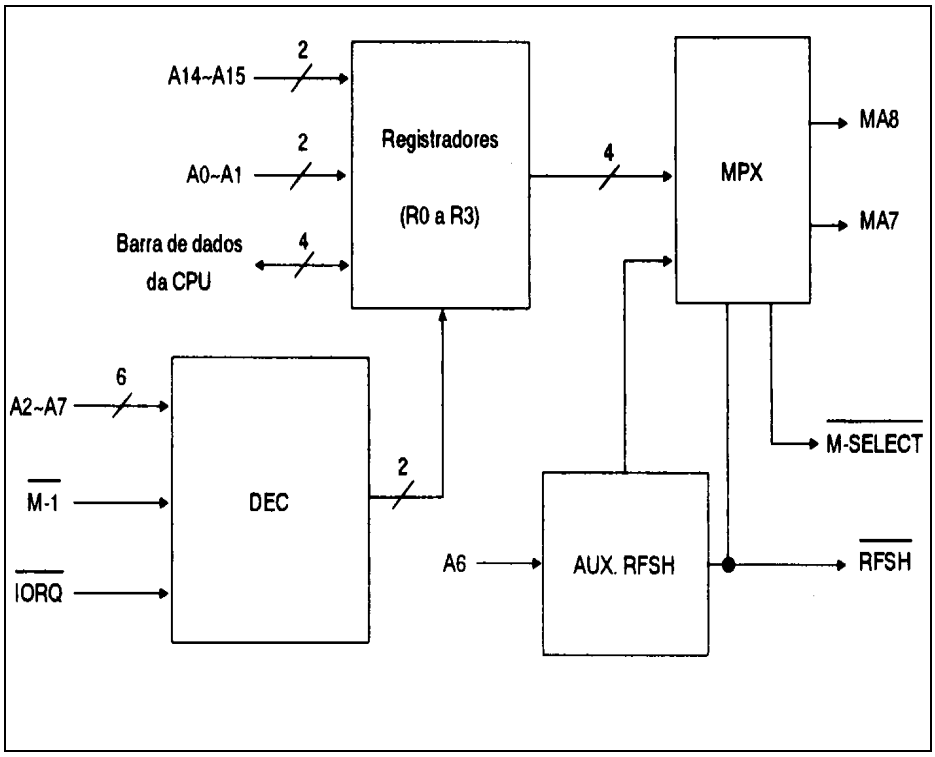

Illustration 1: The design in Blocks

Z80, when running a reading operation or writing (IN/OUT) in the ports of numbers &HFC &HFF, does with that the decoder (Dec) it sends a signal of logic " level 0 " for the records of Mapper, allowing these to be accessed by Z80.
When these records are not being accessed by Z80 become selected by the lines of addresses A15 A14 and the data contained in these are correspondents to the multiplexador (MPX) that transform them in lines of addressing multiplexadas MA8 and MA7, that are also integral part of the auxiliary circuit of refresh.
The bank of 256 Kbyte is constituted by eight dynamic rams (41256 or equivalent). These memories are characterised by the temporary storage of the data (for fractions of seconds), being necessary that it is made a periodically "refresh" before the data get lost. For this Refresh exists. Z80 possesses a circuit of Refresh that provides an internally "refresh" of up to 64Kbytes. The auxiliary refresh circuit (AuxRfsh) he/she does with that this he/she extends until 256 Kbyte.

PART 2 - THE IMPLEMENTATION OF THE HARDWARE

In the Illustration 4 we have the schema of Mapper. He is very simple and for quite so Mapper can be assembled in a board standard, that you/they are those boards that already come with holes and islands, own for experimental assemblies and that you/they are easily found at the stores of electronic material.

We should append to the assembly a " flat cable " of 50 roads (used cable us for connection of printers, drive interfaces etc.) And a connector of the New type " Latch " of 50 roads, what allows our board to be connected in the Bus Expansion, reducing like this the only three the number of threads the they be soldiers in the main board of the personal computer.
Memory Mappers installed internally that you/they were the sale in the national market used this system, what facilitated his/her installation and an eventual maintenance.
We didn't advise Memory Mapper's assembly for people that don't have a certain knowledge in electronics and practice in assemblies. Not because the circuit is complex, more yes for the risks of damages to the personal computer, in case it is made some wrong link in the board of Mapper, since she will be linked to the data bus and addressing of the system. In these buses they are, among other components, VDP (V9938 for MSX2 or V9958 for MSX2+) and the clock (RP 5C01) that, if they are damaged, difficulty they can be substituted.

If you don't possess background with electronic assemblies, don't lose hope: call some friend, relative or neighbour with knowledge in the area.

2.1) THE ILLUSTRATIONS

The Illustration 4, as mentioned, it is the schema of our Memory Mapper. In her they are the links between CIs and the names of the used signals. Notice that beside each signal it exists, between parentheses, a number preceded by the letter " P ". They are to indicate in that pin in the Bus Expansion can obtain such signals, for instance:
(P18) A15
This means that the signal A15 is present in Bus Expansion pin 18.
The Illustration 3 presents the disposition of the pins in the Bus Expansion and the Table 1 display Bus Expansion pinagem.
Already the Illustration 2 demonstrates the correct form of accomplishing the links among the signals MA7 and MA8 and M-Select, that should be done directly in the main board of the personal computer. Finally, we included the location of the bank of original RAM (64Kb).

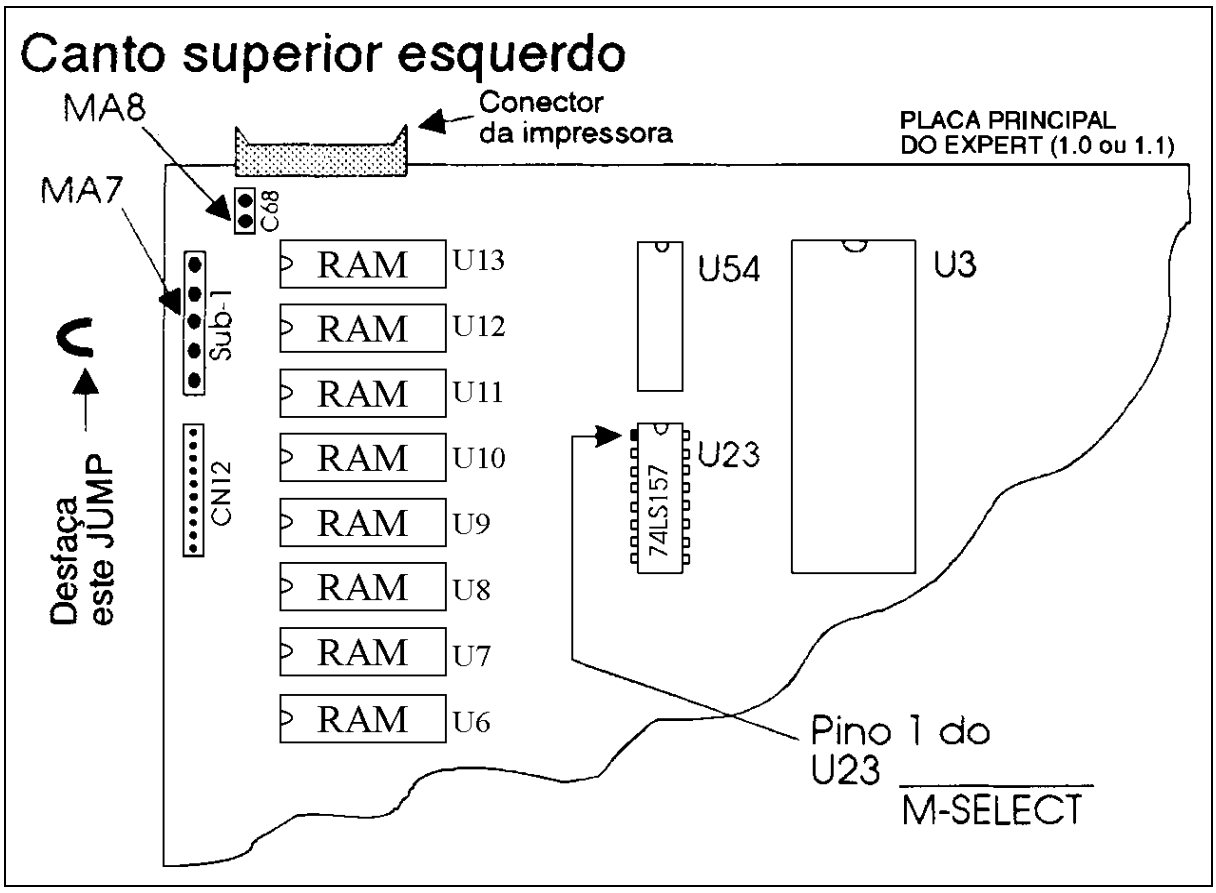

Illustration 2: The motherboard of Expert

2.2) CLUES FOR ASSEMBLY

The board for the assembly should not exceed the size of 10 cm x 7 cm, that are dimensions more than enough for the assembly and it can be easily seated inside of the personal computer.
Mount Bus Expansion connector, that is, the "flat cable" and the "new latch" (connector).
Unbundle the threads of the flat cable in pairs and odd - this will facilitate the welding of the cable the board of Mapper and the identification of Bus Expansion signals.
Weld the connector of Mapper.
Dispose and weld CIs in the board of mode Mapper to facilitate to the maximum the links that will must done among them.
Make the links of GNDs of CIs with GND of the cable of the connector (P41) and (P43).
Check.
Make the links of the pin +5 volts of CIs with the thread 5 volts of the cable of the connector (P45) and (P47).
Check.
Make the links between CIs and the links of CIs and the cable of the connector.
Check, reconfirm and check again. This is the most delicate part of the assembly; therefore every care is needed.

2.3) TESTS

Before starting the tests, disconnect all and any interface or cartridge that it be bound to the personal computer.

With the assembly very well checked, dock the connector of the board in the Bus Expansion and start the personal computer. If the personal computer locks or does not boot, check everything again.

To be sure everything is well, shut down the personal computer and make the links of the signals MA7, MA8 and M-Select with the backup of the illustration 4. Start the personal computer again and if the personal computer locks or does not boot, check everything again.

Everything being right, still with backup of the illustration 4; substitute the bank of RAM 64k for the 256k bank. If it doesn't boot or lock, verify the 256K bank. With certainty there are no more defective memories or with kneaded pins.

Everything OK? Then we are going to the final test: connect the drive interface and load some game of MegaRAM adapted for Mapper (preferably a 256Kb game as it is the case of Xevious, Space Mambow, Nemesis III, among other).

If the game turns, congratulations, you got to assemble his/her Mapper correctly and now it is enoughto install her definitively of the personal computer. Otherwise, don't lose hope. Try other games, because there is always the possibility of the game to be defective, but if none works, well... check everything again! With certainty there is something wrong!

Don't worry about errors project. We have a same Mapper as this installed in our personal computers for about two years and we have not had any problems.

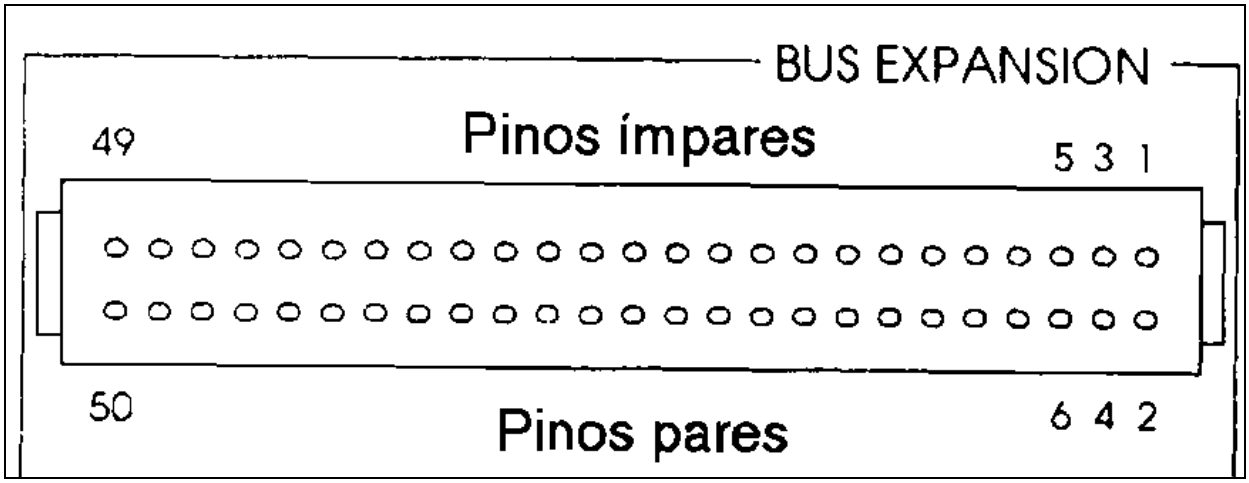

Illustration 3: The disposition of BUS Expansion pins

Table 1: PINS OF THE SLOTS AND OF THE BUS EXPANSION

PIN	I/O	I/O	NAME	DESCRIPTION
01	O		CS1	Chip select of ROM 4000-7FFF
02	O		CS2	Chip select of ROM 8000-BFFF
03	O		CS1/2	Chip select of ROM 4000-BFFF
04	O		SLTSL	Selection of the slot
05	-		Reserve.	Reserved for future use
06	O		RSFH	Refresh signal
07	I		WAIT	Wait signal for CPU
08	I		INT	Signal to request interrupt
09	O		M1	Signal of the 1st cycle of the fetch
10	I		BUSDIR	Control of the direction of the buffer of the BUS
11	O		IORQ	Signal of interrupt of I/O
12	O		MERQ	Signal of request of memory
13	O		WR	Writing signal
14	O		RD	Reading signal
15	O		RESET	Signal of reset of the system
16	-		Reserve.	Reserved for future use
17	O		A9	Bus of addresses
18	O		A15	Bus of addresses
19	O		A11	Bus of addresses
20	O		A10	Bus of addresses
21	O		A7	Bus of addresses
22	O		A6	Bus of addresses
23	O		A12	Bus of addresses
24	O		A8	Bus of addresses
25	O		A14	Bus of addresses
26	O		A13	Bus of addresses
27	O		A1	Bus of addresses
28	O		A0	Bus of addresses
29	O		A3	Bus of addresses
30	O		A2	Bus of addresses
31	O		A5	Bus of addresses
32	O		A4	Bus of addresses
33	I/O		D1	Bus of data
34	I/O		D0	Bus of data
35	I/O		D3	Bus of data
36	I/O		D2	Bus of data
37	I/O		D5	Bus of data
38	I/O		D4	Bus of data
39	I/O		D7	Bus of data
40	I/O		D6	Bus of data
41	-		GND	Earth
42	-		CLOCK	Clock of CPU (3.575.611Hz)
43	-		GND	Earth
44	-		SW1	Switch of Protection
45	-		+5V	+5V
46	-		SW2	Switch of Protection
47	-		+5V	+5V
48	-		+12V	+12V
49	|		SOUNDIN	Sound Input
50	-		-12V	-12V

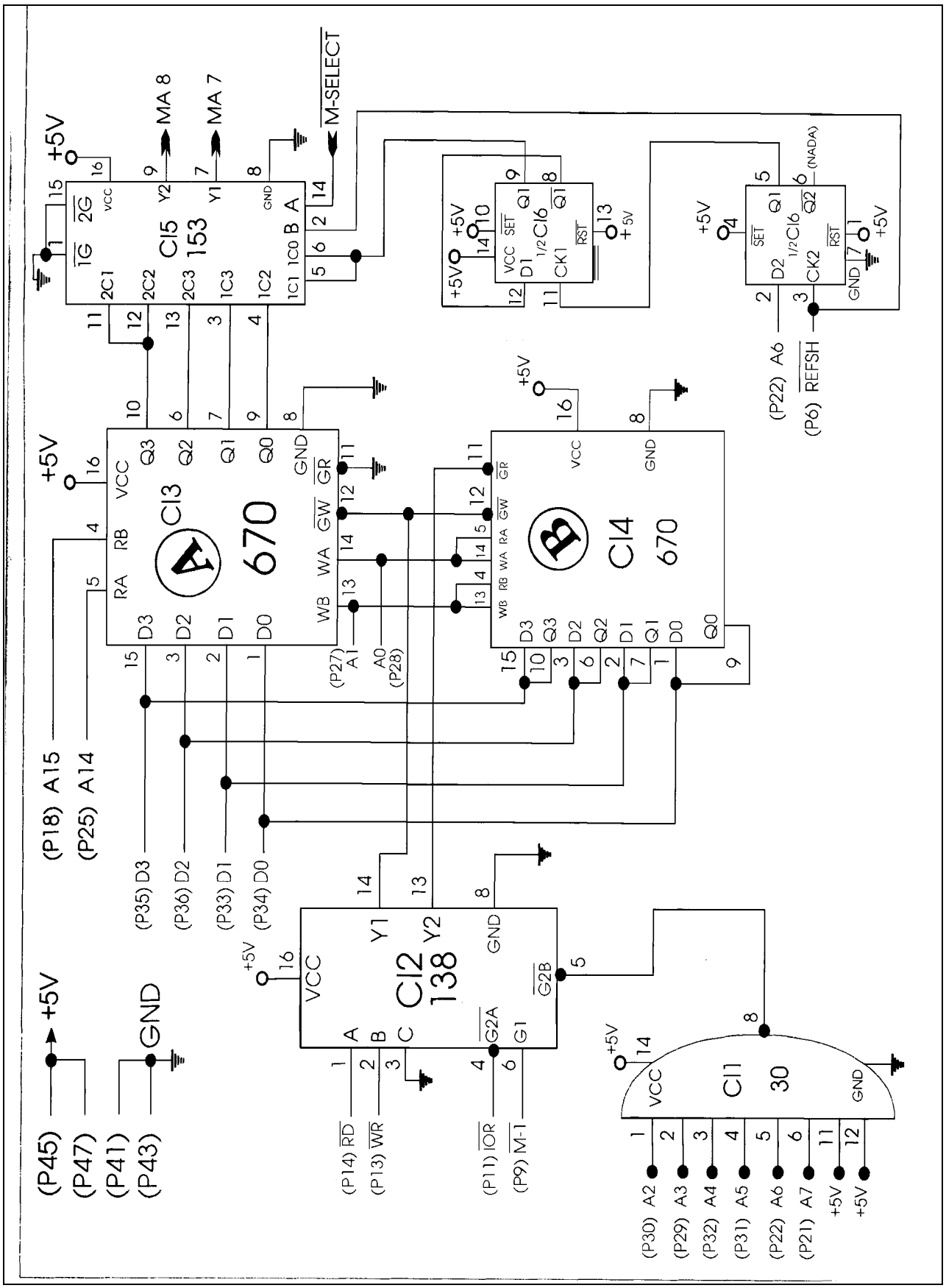

Illustration 4: Memory Mapper's Schema